REMARKS

Claims 9-105 were rejected under the judicially created doctrine of double patenting as being unpatentable over prior U.S. Patent No. 5,794,003. Thus, in response, Applicants submit the attached terminal disclaimer. It is submitted that the Applicant has the right to seek broader claim cover and/or claim coverage for different aspects of the invention in a continuation application.

Claims 49-60, 62-64, 75, 77-78, and 92-105 were rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa et al. Claims 61, 65-66, 71-74, and 79-91 were rejected under 35 U.S.C. 103 as being unpatentable over Ishikawa et al. in view of Rustad et al.

I. Formal Matters

Claims 92 and 101 were amended for grammatical and stylistic purposes. Such amendments should not be interpreted as narrowing the scope of the pending claims in light of the cited references, unless otherwise explicitly indicated and argued below.

II. The Present Invention

The present invention relates to systems and methods for increasing the speed of execution of instructions. More particularly, the present invention relates to a computing system architecture where groups of instructions are stored in parallel and where instructions are issued both sequentially and in parallel.

One embodiment of the present invention is illustrated in Fig. 3. As illustrated, register 130 stores groups of instructions, for example Group 1 and Group 2. The instructions W0, W1, and W2 in Group 1 are to be issued in parallel to pipelines 1, 2, and 3, respectively; and the instructions W2, W3, and W4 in Group 2 are to be issued in parallel to pipelines 1, 3, and 6, respectively. In this embodiment, the instructions in Group 1 are issued to the pipelines at a different time than when the instructions in Group 2 are issued to the pipelines. This distinction is reflected in the pending claims.

Claim 49 recites a method for issuing a group of individual instructions in parallel for processing including, among other limitations, storing in parallel a plurality of instructions and instruction grouping information in a location in a memory, the plurality of instructions and the instruction grouping information determined by a compiler, the

instruction grouping information indicating which instructions of the plurality of instructions belong to a first group of instructions and can be issued in parallel, and indicating at least another instruction of the plurality of instructions that can be issued after the first group of instructions.

Claim 63 recites, a computing system including a cache including a plurality of cache entries, a cache entry of the plurality of cache entries configured to store in parallel a plurality of software-scheduled instructions and instruction grouping information, the instruction grouping information configured to identify a first group of software-scheduled instructions from the plurality of software-scheduled instructions and to identify at least another software-scheduled instruction from the plurality of software-scheduled instructions, the at least another software-scheduled instruction to be issued after instructions in the first group of software-scheduled instructions.

Claim 81, as amended, recites a computing system in which instructions are issued in parallel to processing pipelines including, among other limitations, a storage configured to store an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions in the plurality of instructions are included in the group of instructions, the data associated with the plurality of instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at a compile time.

Claim 92, as amended, recites a method for issuing groups of instructions in parallel to processing pipelines including, among other limitations, storing in a storage, an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data associated with the plurality of instructions, the data associated with the

plurality of instructions indicative of which instructions are included in the group of instructions, the data associated with the instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at compile time.

Claim 101, as amended, recites a method of operating a microprocessor including, among other limitations, storing in a memory storage the frame of instructions, the frame of instructions including a plurality of instructions and issue data, the plurality of instructions including at least a first instruction, a second instruction, and a third instruction, the issue data comprising data indicating that the first instruction is to be issued before the second instruction and the third instruction and that the second and third instructions are to be issued in parallel, and the issue data indicating respective processing units appropriate for the first instruction, the second instruction, and the third instruction.

II. The Cited Reference

A. Ishikawa et al.

Ishikawa et al. relates to a parallel pipelined instruction processing system with reduced branch instruction processing delay. The Examiner has cited col. 1, lines 21-47 and col. 10, lines 23-62 as teaching a memory as recited in some of the independent claims. As will be discussed below, the Applicant traverses these assertions.

Col. 1, lines 21-47 of Ishikawa appears to disclose operation of a VLIW type parallel instruction processing system. Ishikawa discloses at compile time, instructions to be processed in parallel are combined and stored in one instruction line. Col. 1, lines 31-34.

Col. 10, lines 23-et seq. appears to disclose an embodiment where a very long instruction word (VLIW) includes a conditional instruction. If a condition is satisfied, the conditional instruction is executed at the same time as the other instructions as the VLIW. If the condition is not satisfied, the conditional instruction is not executed at all.

In particular, Ishikawa illustrates an instruction field 2 that includes instructions 1, 2, 3, and 4. Ishikawa then states that in Fig. 7, instruction 4 is a conditional branch instruction and instruction 2 is executed only when the branch condition is satisfied. Col. 10. lines 63-66. Further, Ishikawa states that if the branch condition is not satisfied, instruction 2

is not executed. Col. 11, lines 4-6. In other words, instructions 1, 2 & 3 are issued in parallel if the condition is satisfied, and instructions 1 & 3 are issued in parallel if the condition is not satisfied. In the latter case, instruction 2 is not executed.

In sum, Ishikawa discloses storing and issuing in parallel, a single group of instructions. Which instructions are included in the single group depends upon branch conditions. Notably, Ishikawa does not disclose storing anything more than a single group of parallel instructions in the memory.

B. Rustad et al.

Rustad et al. relates to a decoded instruction cache with multiple instructions per cache line. The Examiner has cited Fig. 1 in Rustad as teaching a crossbar for routing multiple instructions.

III. Cited Reference Distinguished

In response to the rejections of claims 49-60, 62-64, 75, 77-78, and 92-105 as being anticipated by Ishikawa or obvious in light of Ishikawa and Rustad, the undersigned traverses all of the Examiner's rejections.

A. Claim 49

Ishikawa does not disclose, teach, or suggest all the limitations of Claim 49. For example, Ishikawa does not disclose storing in parallel a plurality of instructions and instruction grouping information in a location in a memory, the plurality of instructions and the instruction grouping information determined by a compiler, the instruction grouping information indicating which instructions of the plurality of instructions belong to a first group of instructions and can be issued in parallel, and indicating at least another instruction of the plurality of instructions that can be issued after the first group of instructions, among other limitations.

As disclosed above, Ishikawa discloses storing only one group of instructions to be issued in parallel per instruction field. In Ishikawa, instructions in the one group without conditions are automatically issued, however instructions that have conditions will either be issued in parallel with the unconditional instructions, or not at all. There is no disclosure in

Ishikawa about storing instructions that can be issued after a first group of instructions, as recited above.

In sum, Ishikawa does not teach at least the above limitation of claim 49. Claim 49 is therefore asserted to be allowable for at least this reason.

B. Claim 63

Ishikawa does not disclose, teach, or suggest all the limitations of Claim 63. For example, Ishikawa does not disclose a plurality of cache entries, a cache entry of the plurality of cache entries configured to store in parallel a plurality of software-scheduled instructions and instruction grouping information, the instruction grouping information configured to identify a first group of software-scheduled instructions from the plurality of software-scheduled instructions and to identify at least another software-scheduled instruction from the plurality of software-scheduled instructions, the at least another software-scheduled instruction to be issued after instructions in the first group of software-scheduled instructions.

As argued above, Ishikawa discloses storing only one group of instructions to be issued in parallel per instruction field. In Ishikawa, instructions in the one group without conditions are automatically issued, however instructions that have conditions will either be issued in parallel with the unconditional instructions, or not at all. There is no disclosure in Ishikawa about another instruction that can be issued after a first group of instructions, as recited above.

In sum, Ishikawa does not teach at least the above limitation of claim 63. Claim 63 is therefore asserted to be allowable for at least this reason.

C. Claim 81

Ishikawa does not disclose, teach, or suggest all the limitations of Claim 81. For example, Ishikawa does not disclose a storage configured to store an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data associated with

the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions in the plurality of instructions are included in the group of instructions, the data associated with the plurality of instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at a compile time.

As argued above, Ishikawa discloses storing only one group of instructions to be issued in parallel per instruction field. In Ishikawa, instructions in the one group without conditions are automatically issued, however instructions that have conditions will either be issued in parallel with the unconditional instructions, or not at all. There is no disclosure in Ishikawa about an instruction frame storing an instruction that can be issued at a time different from a time a group of instructions can be issued, as recited above.

In sum, Ishikawa does not teach at least the above limitation of claim 81. Claim 81 is therefore asserted to be allowable for at least this reason.

D. Claim 92

Ishikawa does not disclose, teach, or suggest all the limitations of Claim 92. For example, Ishikawa does not disclose storing in a storage, an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions are included in the group of instructions, the data associated with the instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at compile time.

As argued above, Ishikawa discloses storing only one group of instructions to be issued in parallel per instruction field. In Ishikawa, instructions in the one group without conditions are automatically issued, however instructions that have conditions will either be issued in parallel with the unconditional instructions, or not at all. There is no disclosure in

Ishikawa about storing an instruction that can be issued at a time different from a time a group of instructions within the same instruction frame can be issued, as recited above.

In sum, Ishikawa does not teach at least the above limitation of claim 92. Claim 92 is therefore asserted to be allowable, for at least this reason.

E. Claim 101

Ishikawa does not disclose, teach, or suggest all the limitations of Claim 101. For example, Ishikawa does not disclose storing in a memory storage the frame of instructions, the frame of instructions including a plurality of instructions and issue data, the plurality of instructions including at least a first instruction, a second instruction, and a third instruction, the issue data comprising data indicating that the first instruction is to be issued before the second instruction and the third instruction and that the second and third instructions are to be issued in parallel, and the issue data indicating respective processing units appropriate for the first instruction, the second instruction, and the third instruction.

As argued above, Ishikawa discloses storing only one group of instructions to be issued in parallel per instruction field. In Ishikawa, instructions in the one group without conditions are automatically issued, however instructions that have conditions will either be issued in parallel with the unconditional instructions, or not at all. There is no disclosure in Ishikawa about indicating that an instruction can be issued before two other instructions within the same frame of instructions, as recited above.

In sum, Ishikawa does not teach at least the above limitation of claim 101. Claim 101 is therefore asserted to be allowable, for at least this reason.

F. Remaining claims

Claim 49 is asserted to be allowable for the above reasons. Claims 50-62, 77 dependent on claim 49, are also asserted to be allowable for similar reasons as claim 49 and for the additional limitations they recite.

Claim 63 is asserted to be allowable for the above reasons, among others. Claims 64-76 and 78-80, dependent from claim 63, are also asserted to be allowable for similar reasons as claim 63 and for the additional limitations they recite.

Claim 81 is asserted to be allowable for the above reasons among others. Claims 82-91 dependent from claim 81, are also asserted to be allowable for similar reasons as claim 81 and for the additional limitations they recite.

Claim 92 is asserted to be allowable for the above reasons among others. Claims 93-100, dependent from claim 92, are also asserted to be allowable for similar reasons as claim 92 and for the additional limitations they recite.

Claim 101 is asserted to be allowable for the above reasons among others. Claims 102-105, dependent from claim 101, are also asserted to be allowable for similar reasons as claim 101 and for the additional limitations they recite.

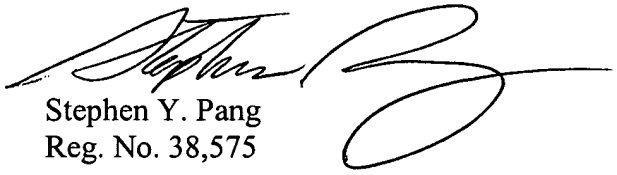
Newly added independent claims 106, 113, 117, 118, 123, 127, and 130 are asserted to be allowable. Further, the respective dependent claims are also asserted to be allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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